LH532000B-S

CMOS 2M (256K × 8/128K × 16)
3 V-Drive Mask-Programmable ROM

FEATURES

- 262,144 words × 8 bit organization
  (Byte mode)
  131,072 words × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access times:
  500 ns (MAX.) at 2.6 V ≤ V_{CC} < 4.5 V
  150 ns (MAX.) at 4.5 V ≤ V_{CC} ≤ 5.5 V
- Static operation
- Three-state outputs
- Low-power supply: 2.6 to 5.5 V
- Programmable OE/$\overline{\text{OE}}$ and OE_1/$\overline{OE_1}$/DC
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)

DESCRIPTION

The LH532000B-S is a CMOS 4M-bit mask-programmable ROM organized as 262,144 × 8 bits (Byte mode) or 131,072 × 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin.

It is suited for use in compact battery back-up systems due to be operated on 3 V power supply.

PIN CONNECTIONS

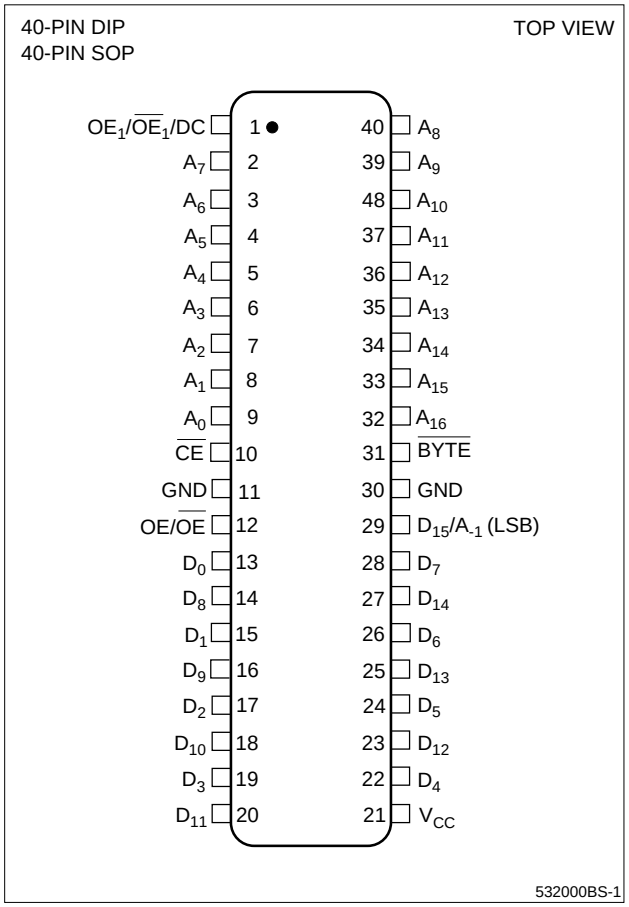


Figure 1. Pin Connections for DIP and SOP Packages

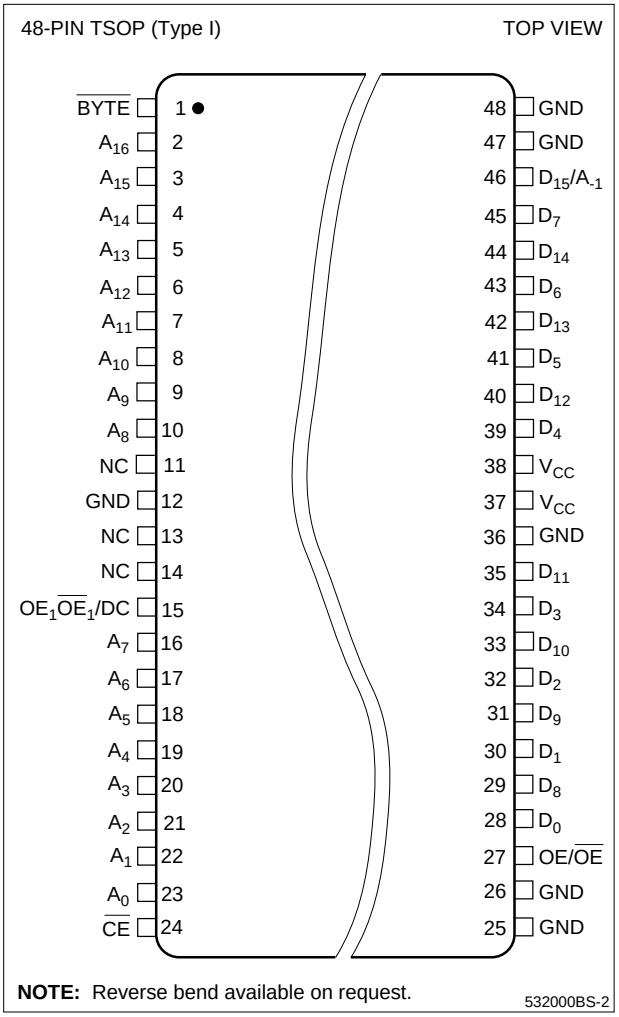


Figure 2. Pin Connections for TSOP Package

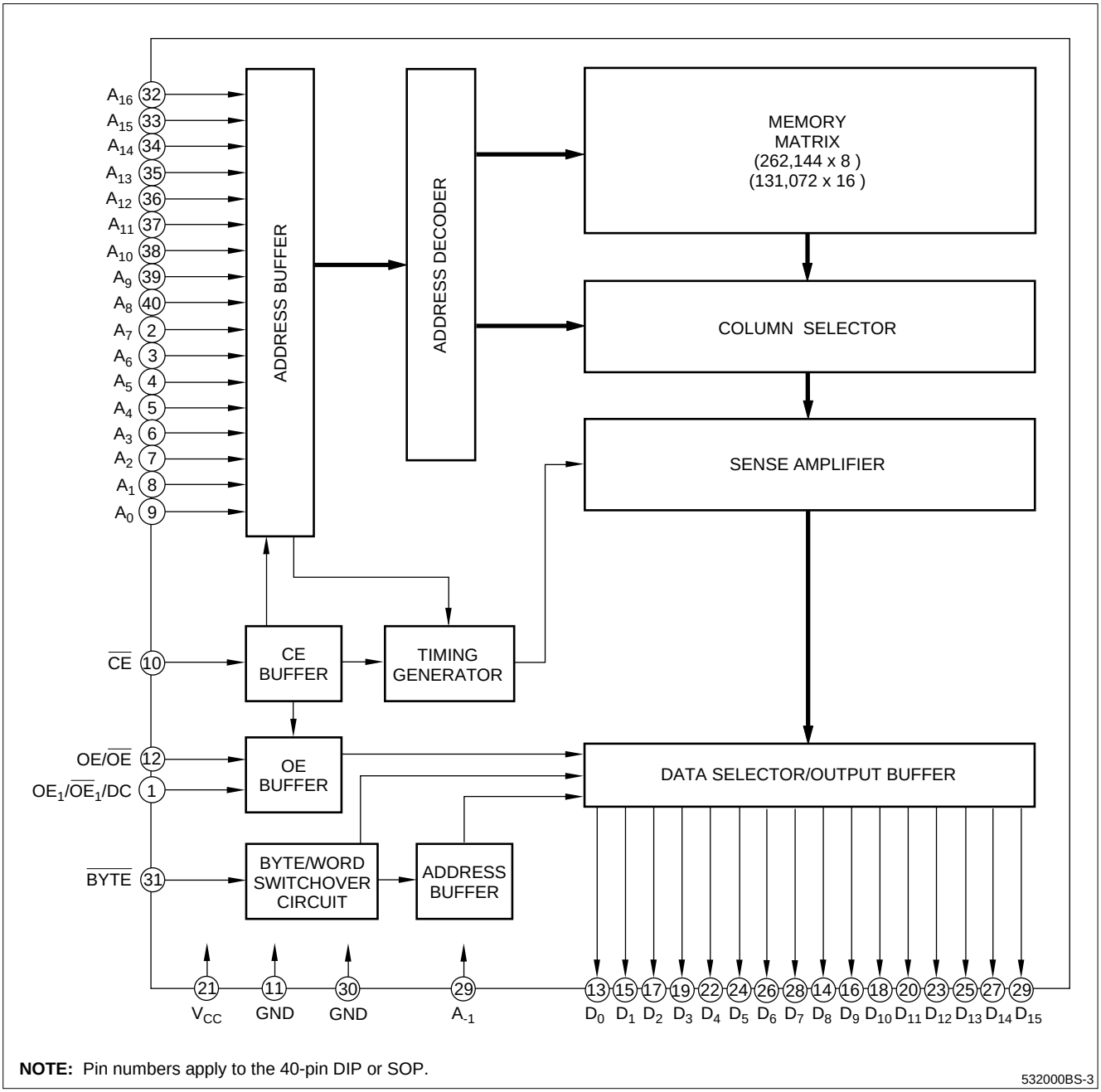


Figure 3. LH532000B-S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
$A_{-1} – A_{16}$	Address input	1
$D_0 – D_{15}$	Data output	1
$\overline{BYTE}$	Byte/word mode switch	1
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	2
$OE_1/\overline{OE}_1$/DC	Output enable input	2, 3
V_{CC}	Power supply	
GND	Ground	

NOTES:

1. The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be LOW in byte mode, and data output (D_{15}) when set to be HIGH in word mode.
2. Active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE}_1$/DC are mask-programmable.
3. DC = Don't care.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE}_1$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
					$D_0 – D_7$	$D_8 – D_{15}$	LSB	MSB	
H	X	X	X	X	High-Z	High-Z	–	–	Standby
L	L/H	X	X	X	High-Z	High-Z	–	–	Operating
L	X	L/H	X	X	High-Z	High-Z	–	–	Operating
L	H/L	H/L	H	–	$D_0 – D_7$	$D_8 – D_{15}$	A_0	A_{16}	Operating
L	H/L	H/L	L	L	$D_0 – D_7$	High-Z	A_{-1}	A_{16}	Operating
L	H/L	H/L	L	H	$D_8 – D_{15}$	High-Z	A_{-1}	A_{16}	Operating

NOTE:
X = H or L, High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.6		5.5	V

DC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}		0.8V_{CC}	V_{CC} + 0.3	V	
Input 'Low' voltage	V_{IL}		–0.3	0.4	V	
Output 'High' voltage	V_{OH}	I_{OH} = –100 µA	0.8V_{CC}		V	
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 500 ns		35	mA	3
	I_{CC3}	t_{RC} = 500 ns		15	mA	4
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} – 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz T_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE}_1$ = V_{IH}, OE/OE_1 = V_{IL}
2. 4.5 V ≤ V_{CC} ≤ 5.5 V, outputs open
3. 3.4 V < V_{CC} < 4.5 V, outputs open
4. 2.6 V ≤ V_{CC} ≤ 3.4 V, outputs open

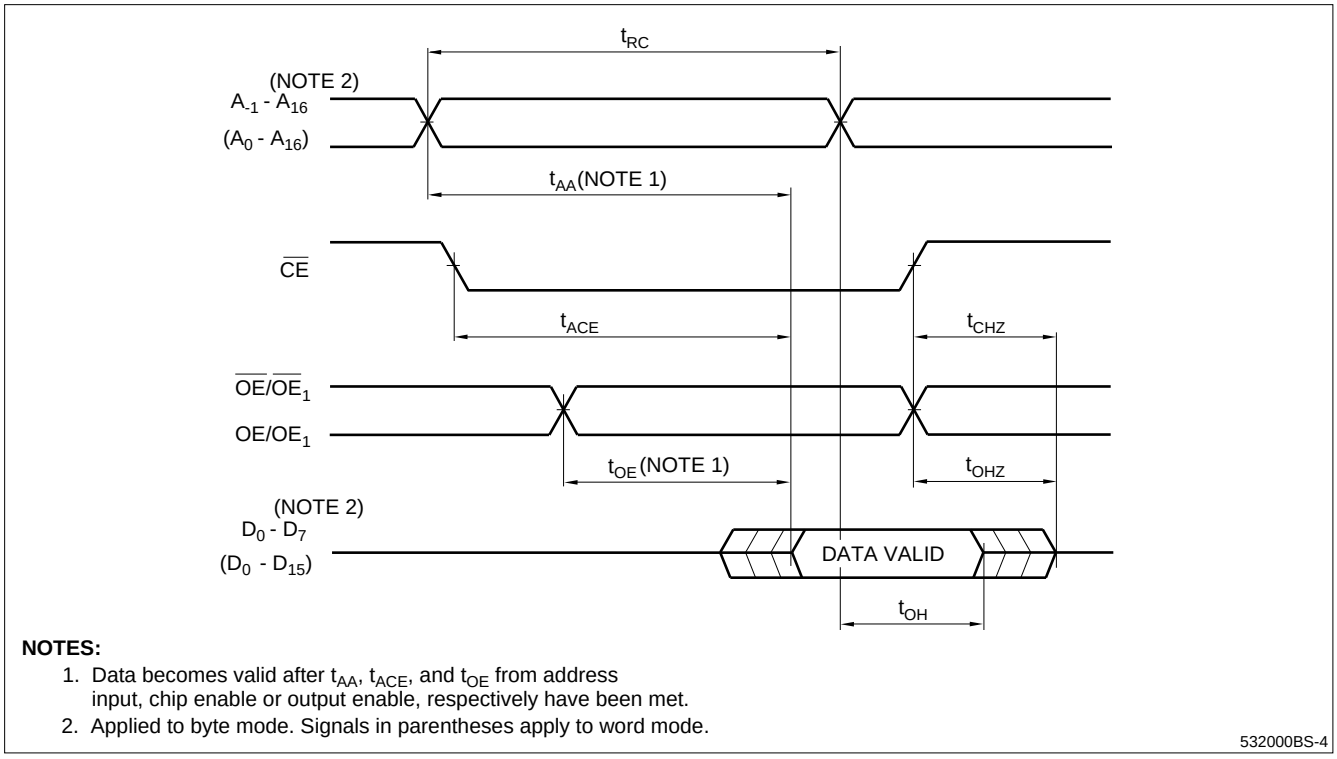
AC CHARACTERISTICS (V_{CC} = 2.6 to 5.5 V, T_A = 0 to +70°C)

PARAMETER	SYMBOL	2.6 ≤ V_{CC} < 4.5		4.5 ≤ V_{CC} ≤ 5.5		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	500		150		ns	
Address access time	t_{AA}		500		150	ns	
Chip enable time	t_{ACE}		500		150	ns	
Output enable time	t_{OE}		150		80	ns	
Output hold time	t_{OH}	10		10		ns	
CE to output in High-Z	t_{CHZ}		150		80	ns	1
OE to output in High-Z	t_{OHZ}		150		80	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.4 to (0.8 × V_{CC}) V
Input rise/fall time	10 ns
Input/output reference level	1.5 V
Output load condition	1 TTL + 100 pF



NOTES:
1. Data becomes valid after t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.
2. Applied to byte mode. Signals in parentheses apply to word mode.

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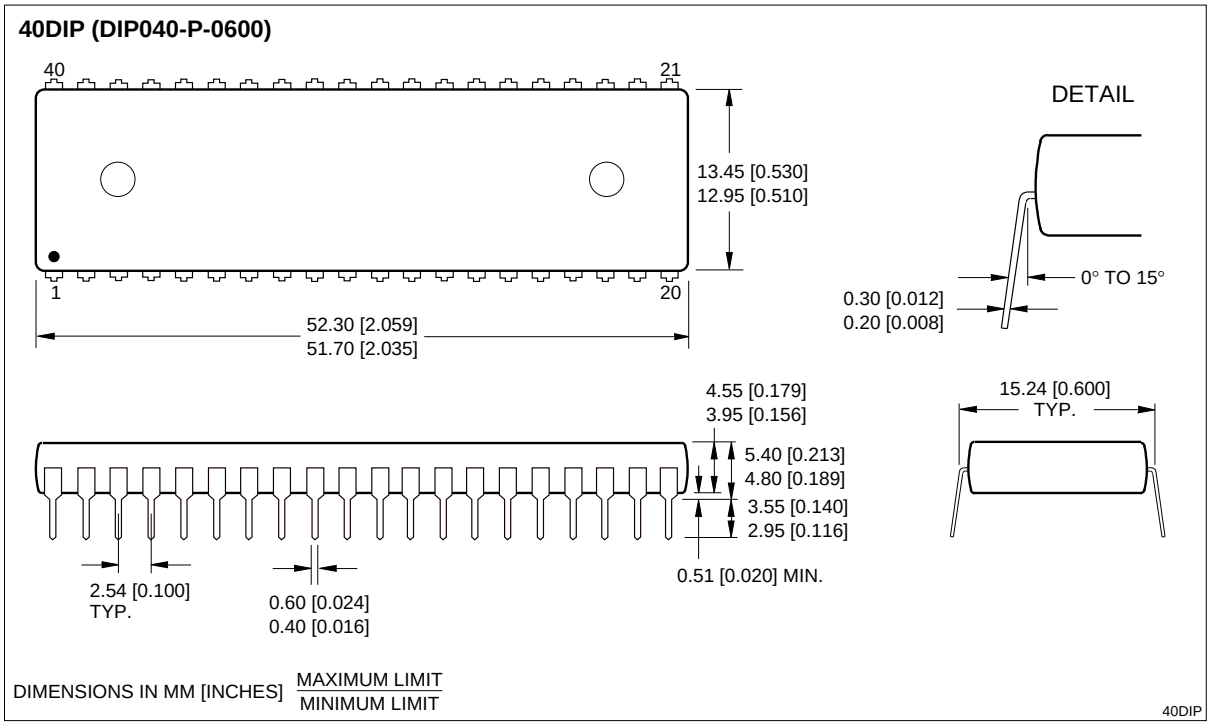
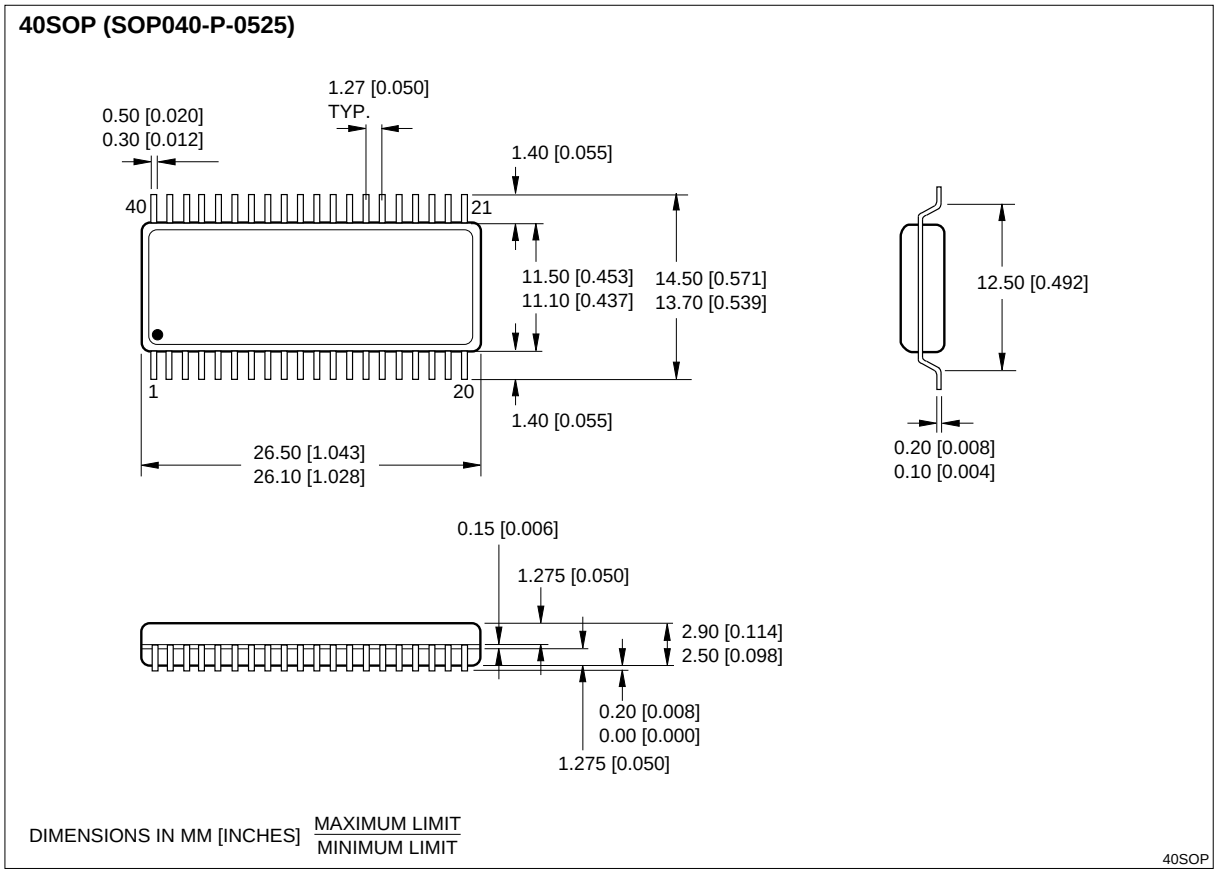
Figure 4. Timing Diagram

PACKAGE DIAGRAMS

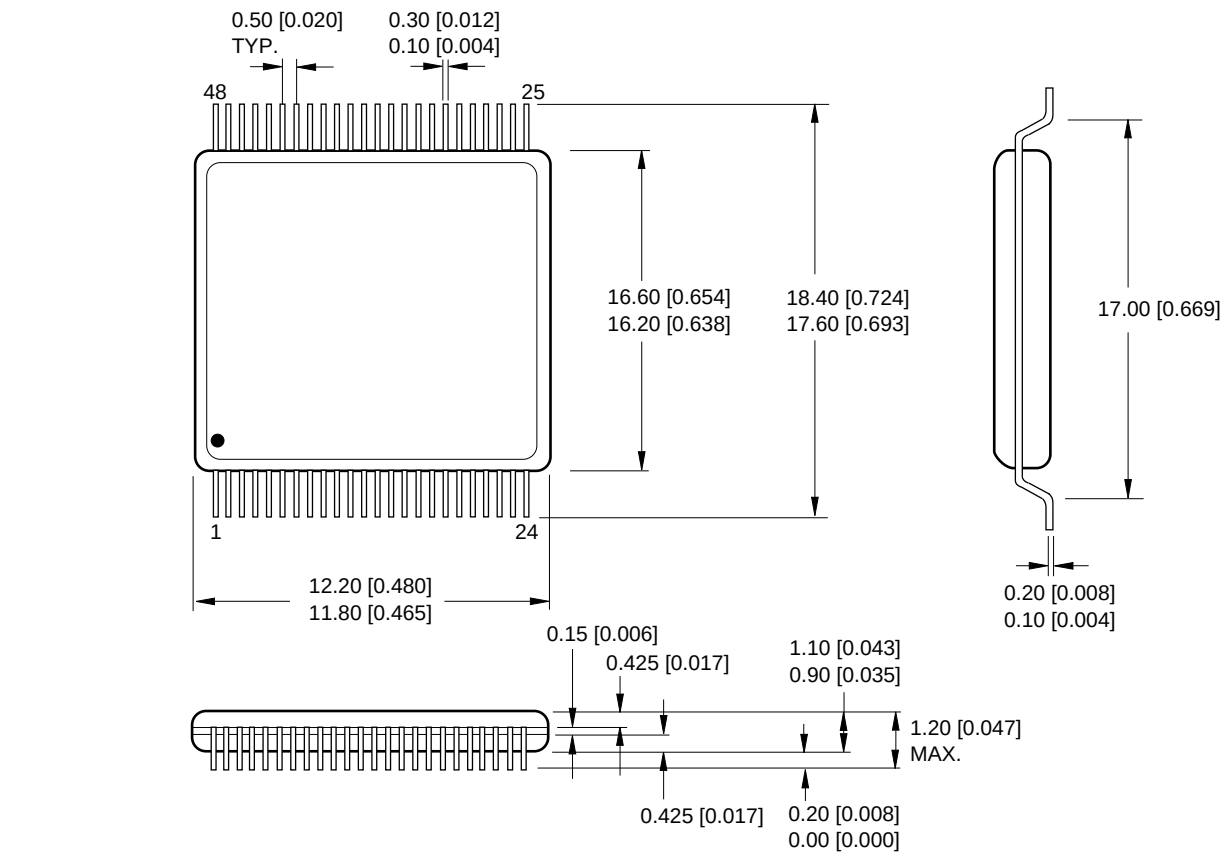


40-pin, 600-mil DIP



40-pin, 525-mil SOP

48TSOP (TSOP048-P-1218)



48-pin, 12 × 18 mm^2 TSOP (Type I)

ORDERING INFORMATION

LH532000B	X	- S
Device Type	Package	Low-Voltage Operation

- D 40-pin, 600-mil DIP (DIP040-P-0600)
- N 40-pin, 525-mil SOP (SOP040-P-0525)
- T 48-pin, 12 x 18 mm^2 TSOP (Type I) (TSOP048-P-1218)
- TR 48-pin, 12 x 18 mm^2 TSOP (Type I) Reverse bend (TSOP048-P-1218)

CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM

Example: LH532000BD-S (CMOS 2M (256K x 8 or 128K x 16) Mask-Programmable ROM, Low-Voltage Operation, 40-pin, 600-mil DIP)

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